Dual H-Bridge Motor Driver IC

1. Description

The AP8300 provides a dual H-bridge motor driver which wide range of motor power supply voltage from 4.0V to 18.0V and low power consumption at sleep mode. This sleep mode can be set using a dedicated nSLEEP pin.

The ETSSOP Package is most suitable for home appliance and general brushed and Stepper Motors.

A simple PWM interface allows easy interfacing to controller circuits.

These H-bridge drivers are full bridge drivers for brush motor applications. The AP8300 is capable of driving up to 1.0A of current from each output of 2.0A of current in parallel mode (with proper heat sinking, at 12V and T_A=25℃)

Internal protection functions are provided for UVLO, OCP, Short-circuit protection, and overtemperature. Fault conditions are indicated by a nFAULT pin.

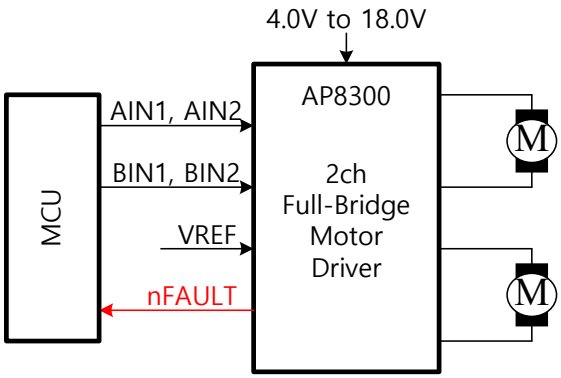
2. Features

- Dual H-Bridge Motor Driver
  - Single/Dual Brushed DC
  - Stepper
- PWM Control Interface
- Optional Current Regulation With 20.0μs Fixed Off-Time
- High Output Current per H-Bridge
  - 1.0A Maximum Driver Current at 12 V and T_A = 25°C
  - Parallel Mode Available Capable of 2.0A Maximum Driver Current at 12 V and T_A = 25°C
- 4.0V to 18.0V Operating Supply Voltage Range
- Low-Current 3.0μA Sleep Mode
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

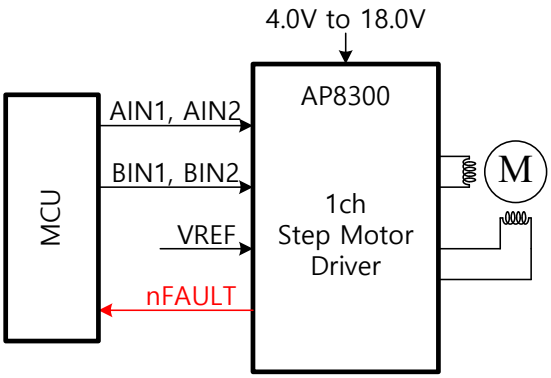
3. Applications

- Home Appliances
- Refrigerator, damper
- General Brushed and Stepper Motors
- Laser Printer, Inkjet Printer, Photo Printer
- Photo Printer, Mini Printer

Simplified Schematic1



Simplified Schematic2



4. Pin Configuration and Description

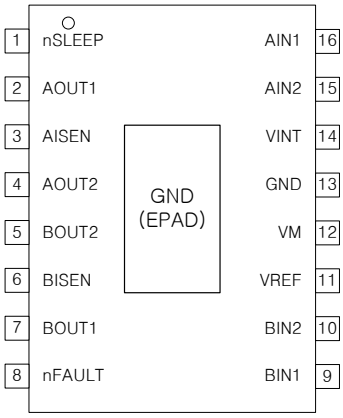


Figure 4-1. Pin Configuration

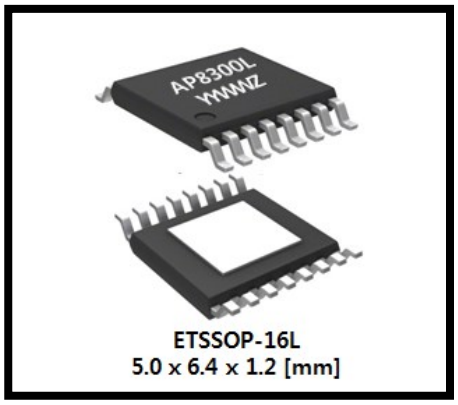


Figure 4-2. Sample Figures

Pin Description

PKG PAD No.	PKG PIN Assignment	I/O	DESCRIPTION
1	nSLEEP	INPUT	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
2	AOUT1	OUTPUT	Winding A output
3	AISEN	OUTPUT	Connect to current sense resistor for bridge A, or GND if current regulation is not required
4	AOUT2	OUTPUT	Winding A output
5	BOUT2	OUTPUT	Winding B output
6	BISEN	OUTPUT	Connect to current sense resistor for bridge A, or GND if current regulation is not required
7	BOUT1	OUTPUT	Winding B output
8	nFAULT	OUTPUT (Open-Drain)	Connect to current sense resistor for bridge A, or GND if current regulation is not required
9	BIN1	INPUT	Controls BOUT1; internal pulldown
10	BIN2	INPUT	Controls BOUT2; internal pulldown
11	VREF	INPUT	Voltage on this pin sets the full scale chopping current; short to VINT if not supplying an external reference voltage
12	VM	Power	Connect to motor power supply; bypass to GND with a 0.1uF and 10μF (minimum) ceramic capacitor rated for VM
13	GND	GND	Both the GND pin and device PowerPAD must be connected to ground
14	VINT	-	Internal supply voltage; bypass to GND with 2.2μF, 6.3V capacitor
15	AIN2	INPUT	Controls AOUT2; tri-level input
16	AIN1	INPUT	Controls AOUT1; tri-level input

5. Block Diagram

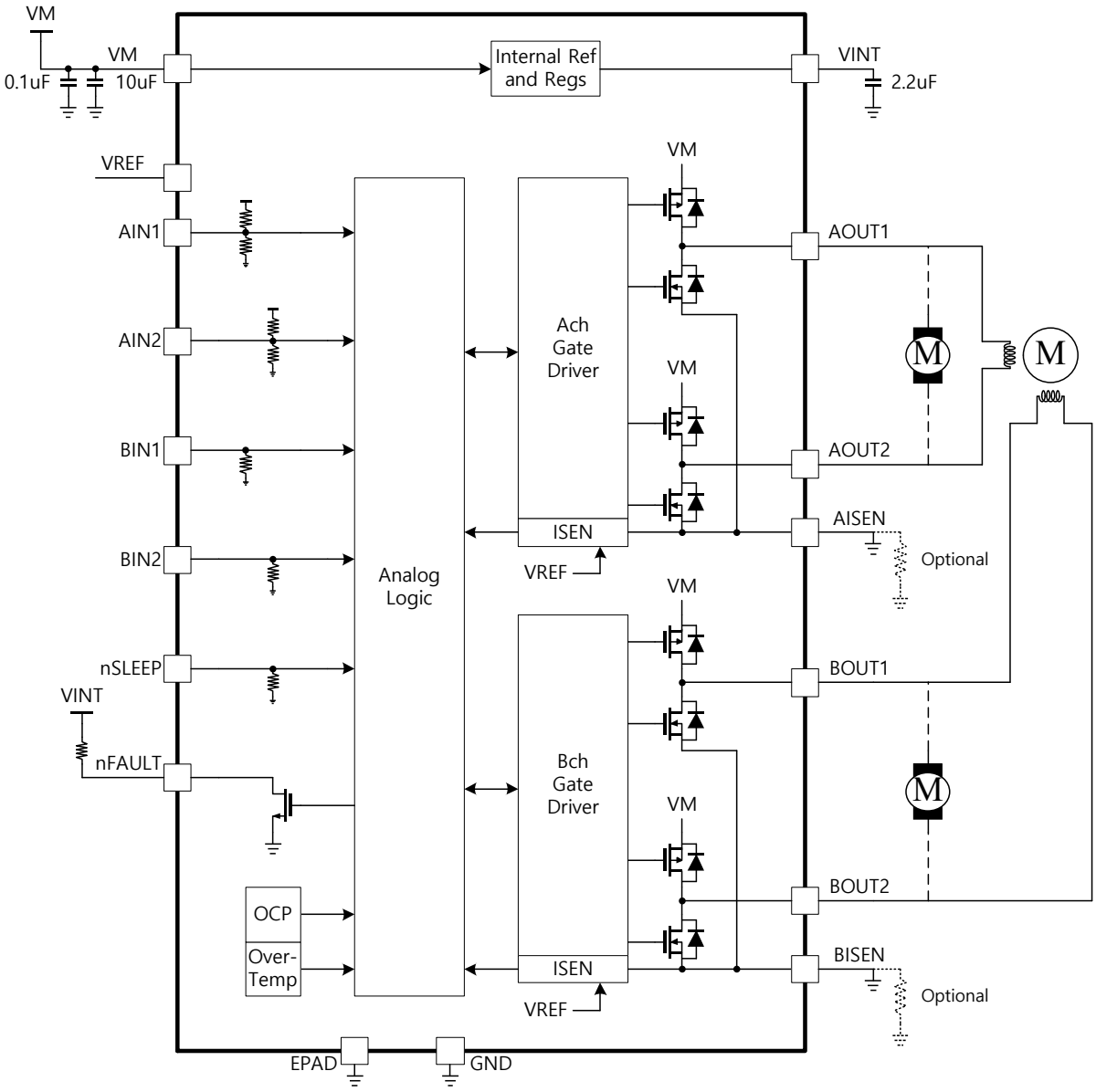


Figure 5-1. Block Diagram

6 Specifications

6.1 Maximum Ratings Characteristics

(T_A = 25℃ unless otherwise specified)

Characteristics		Symbol	Value	Unit
Power supply voltage		VM	-0.3 ~ 20.0	V
Power supply voltage ramp rate		VM_ramp	2.0	V/us
Internal regulator voltage		VINT	3.6	V
Analog input pin voltage		VREF	3.6	V
Control pin voltage		AIN1,AIN2,BIN1,BIN2,nSLEEP, nFAULT	7.0	V
Continuous phase node pin voltage		AOUT1,AOUT2,BOUT1,BOUT2	VM+0.6	V
Continuous shunt amplifier input pin voltage		AISEN, BISEN	0.6	V
Peak drive current		AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN	Internally limited	A
Power dissipation	ETSSOP-16L	PD_ETSSOP_16L	2.8	W
Operating Junction temperature		Topr	-40~150	℃
Storage temperature		Tstg	-55~150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable.

6.2 ESD Rating

Characteristics		Value	Unit
Electrostatic discharge	HBM : Human body model (Ref : JS-001)	±4000	V
	CDM : Charged Device Model (Ref : JS-002)	±1500	

6.3 Recommended Operating Conditions

(T_A = 25℃ unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply voltage range(1)	V_{VM}	4.0	12.0	18.0	V
Reference rms voltage range(2)	V_{REF}	1.0	-	3.3	V
Applied STEP Signal	f_{PWM}	0	-	250	kHz
VINT external load current	I_{VINT}	0	-	1.0	mA
Motor rms current per H-bridge(3)	I_{RMS}	0	-	0.8	A
Operating ambient temperature	T_A	-40	-	85	°C

(1) Note that $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) Operational at VREF between 0 and 1 V, but accuracy is degraded.
(3) Power dissipation and thermal limits must be observed.

6.4 Electrical Characteristics

(T_A = 25℃, V_{VM} = 12V, unless otherwise specified)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
POWER SUPPLIES (VM, VINT)						
VM operating voltage	V_{VM}	-	4	12	18	V
VM operating supply current	I_{VM}	V_{VM} = 12 V, excluding winding current, nSLEEP = 1	0.5	1.8	3.0	mA
VM sleep mode supply current	I_{VMQ}	V_{VM} = 12 V, nSLEEP = 0	0.5	1.2	3.0	μA
Sleep time	t_{SLEEP}	nSLEEP = 0 to sleep mode	-	-	1.0	ms
Wake time	t_{WAKE}	nSLEEP = 1 to output transition	-	-	1.0	ms
Power-on time	t_{ON}	V_{VM} > V_{UVLO} rising to output transition	-	-	1.0	ms
VINT voltage	V_{INT}	V_{VM} > 4 V, I_{OUT} = 0 A to 1 mA	3.13	3.3	3.47	V
LOGIC-LEVEL INPUTS (BIN1, BIN2, NSLEEP)						
Input logic low voltage	V_{IL}	-	0	-	0.7	V
Input logic high voltage	V_{IH}	-	1.6	-	5.5	V
Input logic hysteresis	V_{HYS}	-	100	-	-	mV
Input logic low current	I_{IL}	V_{xINx} = 0 V	–1.0	-	1.0	μA
Input logic high current	I_{IH}	V_{xINx} = 5 V	1.0	-	30	μA
Pulldown resistance	R_{PD}	BIN1, BIN2	-	200	-	kΩ
		nSLEEP	-	500	-	kΩ
Input deglitch time	t_{DEG}	AIN1 or AIN2	-	400	-	ns
		BIN1 or BIN2	-	200	-	ns
Propagation delay	t_{PROP}	AIN1 or AIN2 edge to output change	-	800	-	ns
		BIN1 or BIN2 edge to output change	-	400	-	ns
TRI-LEVEL INPUTS (AIN1, AIN2)						
Tri-level input logic low voltage	V_{IL}	-	0	-	0.7	V
Tri-level input Hi-Z voltage	V_{IZ}	-	-	1.1	-	V
Tri-level input logic high voltage	V_{IH}	-	1.6	-	5.5	V
Tri-level input hysteresis	V_{HYS}	-	100	-	-	mV
Tri-level input logic low current	I_{IL}	V_{xINx} = 0 V	–30	-	–1	μA
Tri-level input logic high current	I_{IH}	V_{xINx} = 5 V	1.0	-	30	μA
Tri-level pulldown resistance	R_{PD}	To GND	-	170	-	kΩ
Tri-level pullup resistance	R_{PU}	To VINT	-	340	-	kΩ
CONTROL OUTPUTS (NFAULT)						
Output logic low voltage	V_{OL}	I_O = 5 mA	-	-	0.5	V
Output logic high leakage	I_{OH}	V_O = 3.3 V	–1.0	-	1.0	μA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
High-side FET on-resistance	$R_{DS(ON)}$	V_{VM} = 12 V, I = 0.5 A, T_J = 25°C	-	700	-	mΩ
		V_{VM} = 12 V, I = 0.5 A, T_J = 85°C (1)	-	900	-	mΩ
Low-side FET on-resistance	$R_{DS(ON)}$	V_{VM} = 12 V, I = 0.5 A, T_J = 25°C	-	400	-	mΩ
		V_{VM} = 12 V, I = 0.5 A, T_J = 85°C (1)	-	520	-	mΩ
Off-state leakage current	I_{OFF}	V_{VM} = 5 V, T_J = 25°C	–1.0	-	1.0	μA
Output dead time	t_{DEAD}	Internal dead time	-	200	-	ns

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
PWM CURRENT CONTROL (VREF, AISEN, BISEN)						
Externally applied VREF input current	I_{REF}	V_{VREF} = 1 to 3.3 V	-	-	1.0	μA
xISEN trip voltage	V_{TRIP}	For 100% current step with V_{VREF} = 3.3 V	-	500	-	mV
Current sense blanking time	t_{BLANK}	-	-	1.8	-	μs
Current sense amplifier gain	A_{ISENSE}	Reference only	-	6.6	-	V/V
Current control constant off time	t_{OFF}	-	-	20.0	-	μs
PROTECTION CIRCUITS						
VM undervoltage lockout	V_{UVLO}	V_{VM} falling; UVLO report	-	-	2.9	V
		V_{VM} rising; UVLO recovery	-	-	3.0	V
Overcurrent protection trip level	I_{OCP}	-	2.0	-	-	A
Overcurrent deglitch time	t_{DEG}	-	-	2.8	-	μs
Overcurrent protection period	t_{OCP}	-	-	1.6	-	ms
Thermal shutdown temperature	T_{TSD} (1)	Die temperature T_J	150	160	180	°C
Thermal shutdown hysteresis	T_{HYS} (1)	Die temperature T_J	-	50	-	°C
Timing Requirements						
Delay time, BIN1 to BOUT1	t_1	-	100	-	600	ns
Delay time, BIN2 to BOUT1	t_2	-	100	-	600	ns
Delay time, BIN1 to BOUT2	t_3	-	100	-	600	ns
Delay time, BIN2 to BOUT2	t_4	-	100	-	600	ns
Output rise time	t_F	-	50	-	150	ns
Output fall time	t_R	-	50	-	150	ns

(1) These parameters, although guaranteed, are not 100% tested in production.

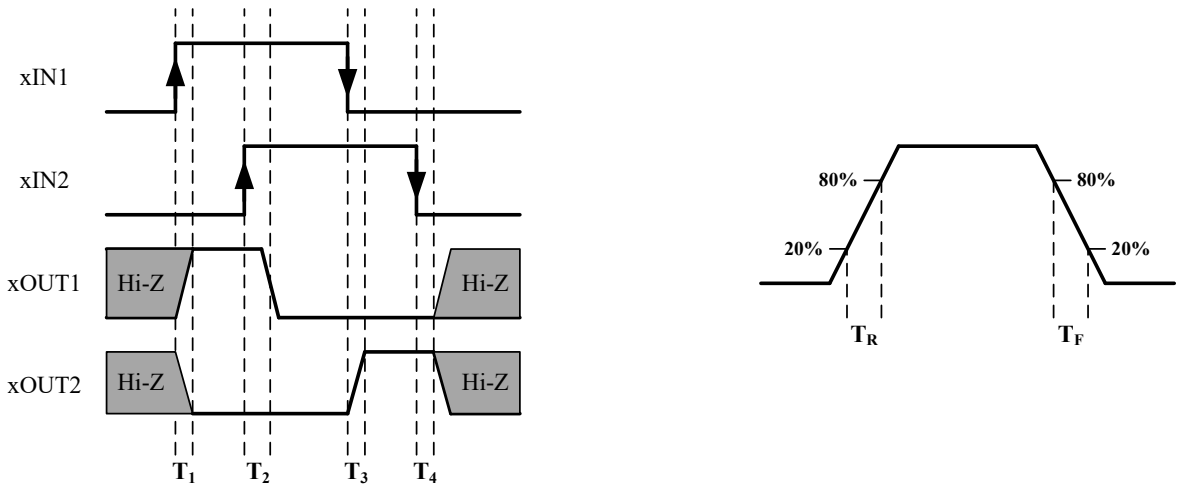


Figure 6-1. Timing Diagram

7. Detailed Description

7.1 Overview

The AP8300 is an integrated motor driver solution for two DC motors or bipolar stepper motors. The device integrates two H-bridges that use an NMOS low-side driver and PMOS high-side driver and current-sense regulation circuitry. The AP8300 can be powered from a supply range of 4.0V to 18.0V and can provide output currents in 0.8A rms.

The simple PWM interface makes it easy to interface with the controller circuitry.

Current regulation uses a fixed off-time (t_{OFF}) PWM scheme. The current-controlled trip point is controlled by the value of the sense resistor and the voltage applied to VREF.

A low-power sleep mode is included that allows the system to save power when the motor is not running.

7.2 Device Functional Modes

The AP8300 is active unless the nSLEEP pin is brought logic low. In sleep mode, the VINT regulator is disabled and the H-bridge FETs are disabled Hi-Z. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The AP8300 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the output change state after wake-up.

When V_{VM} falls below the VM UVLO threshold (V_{UVLO}), the output driver, internal logic, and VINT regulator are reset.

Table 7-1. Functional Modes

MODE	CONDITION	H-BRIDGE	VINT
Operating	4V < V_{VM} < 18V nSLEEP pin = 1	Operating	Operating
SLEEP	4V < V_{VM} < 18V nSLEEP pin = 0	Disabled	Disabled
Fault	Any fault condition met	Disabled	Depends on fault

7.3 Bridge Control

Table 7-2 shows the logic for the inputs xIN1 and xIN2.

Table 7-2. Bridge Control

INPUT			OUTPUT		Function (DC Motor)
NSLEEP	xIN1	xIN2	xOUT1	xOUT2	
1	0	0	Hi-Z	Hi-Z	Coast (Fast decay)
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake (slow decay)

NOTE

Pins AIN1 and AIN2 are tri-level, so when they are left Hi-Z, they are not internally pulled to logic low. When AIN1 or AIN2 are set to Hi-Z and not in parallel mode, the output driver maintains the previous state.

7.4 PWM Motor Drivers

This device contains two identical H-bridge motor drivers with current-control PWM circuitry. Figure 7-1 shows a block diagram of the circuitry.

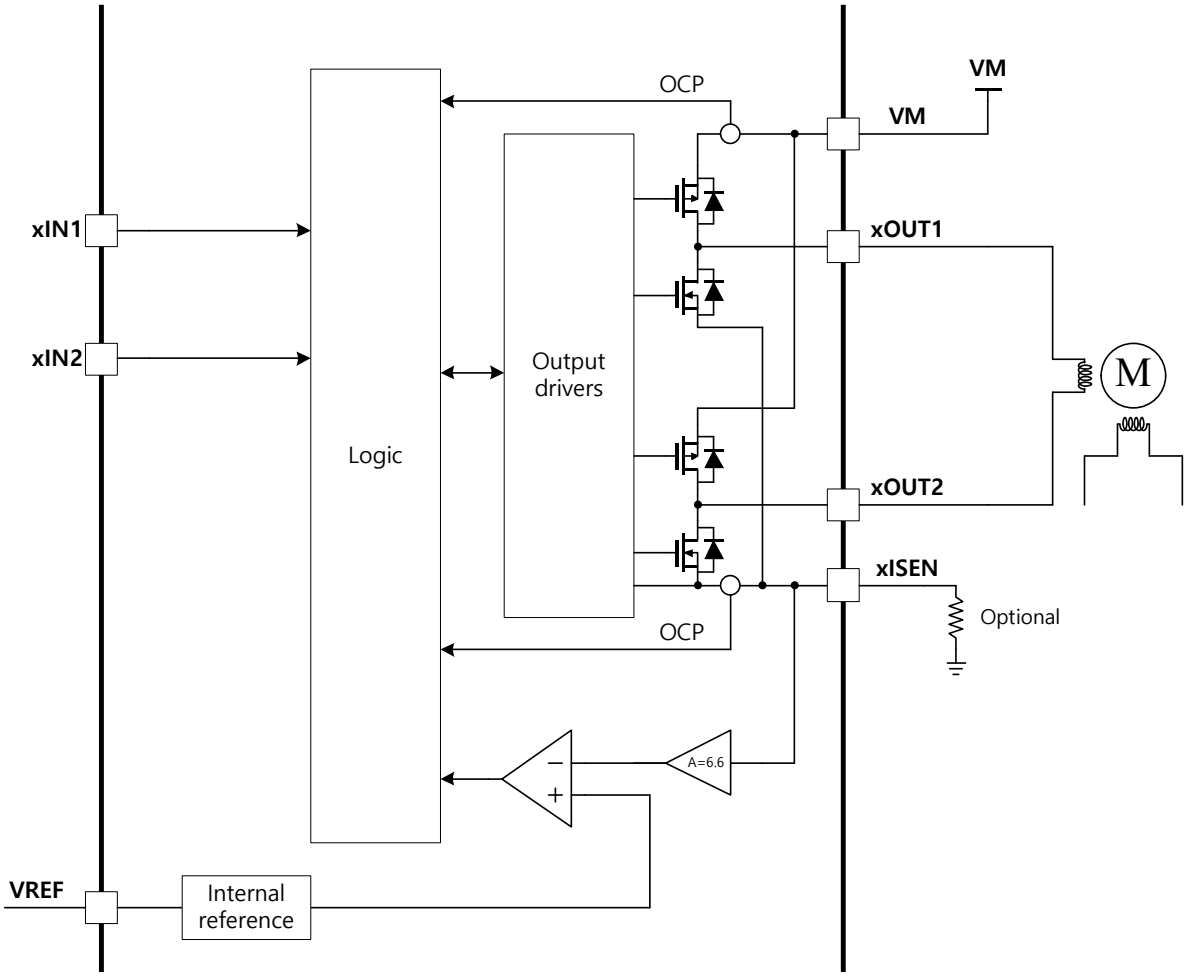


Figure 7-1. PWM Motor Driver Circuitry

7.5 Parallel Operation

Two drivers can be used in parallel to supply twice the current to a single motor. To start parallel mode, Hi-Z must be maintained when AIN1 and AIN2 are powered up or when sleep mode is exited (nSLEEP switches from 0 to 1). BIN1 and BIN2 are used to control the driver. If current control is required, connect AISEN and BISEN to a single sense resistor. To exit the parallel mode, AIN1 and AIN2 must be driven high or low and the device must be powered on or wake-up mode must be exited. Figure 7 shows a block diagram of a device using parallel mode.

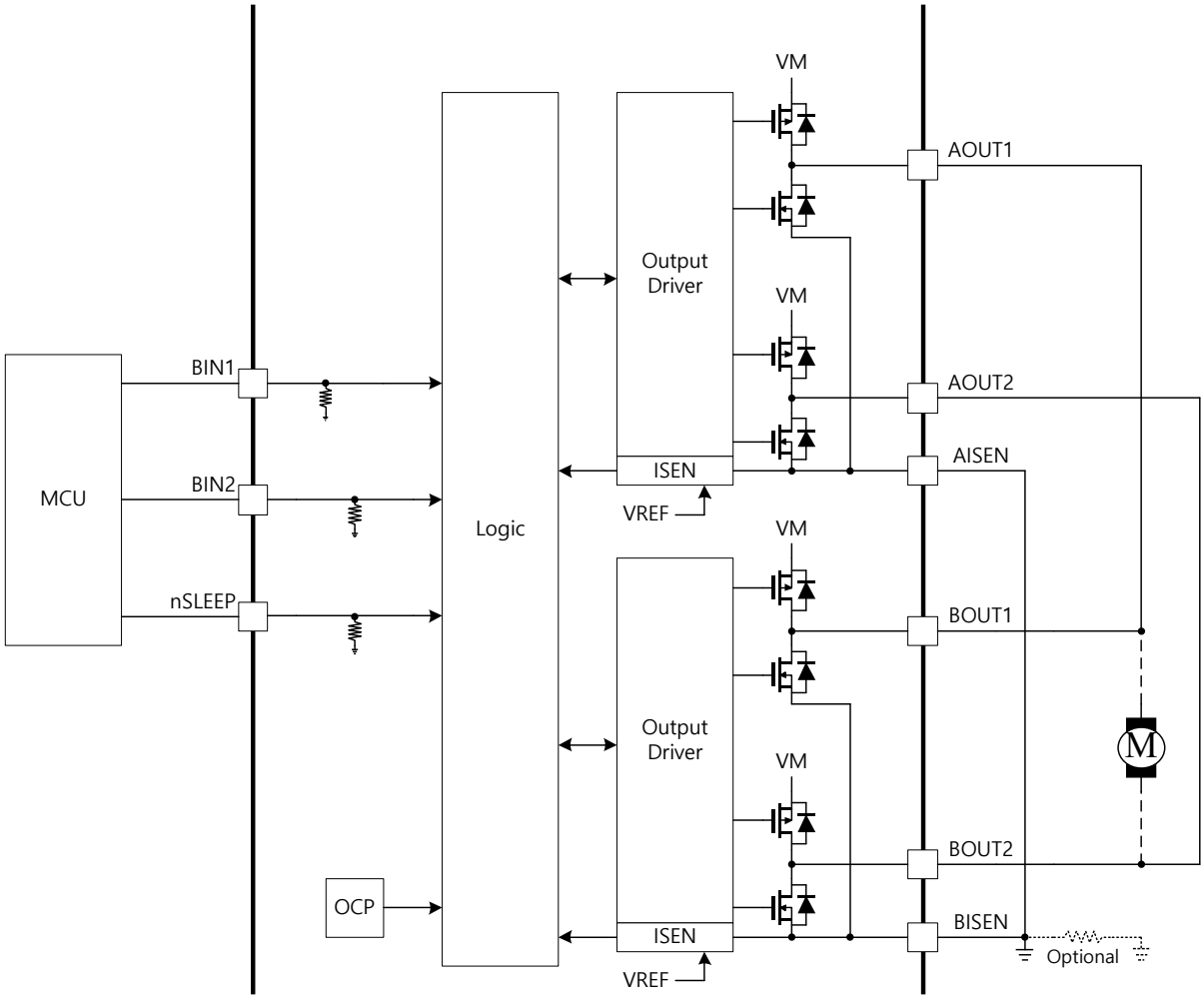


Figure 7-2. Parallel Mode Operation

7.6 Current Regulation

The current through the motor windings is regulated by a fixed-off-time PWM current regulation circuit. With DC brushed motors, current regulation can be used to limit the stall current (which is also the startup current) of the motor.

Current regulation works as follows:
When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current for a time t_{OFF} before starting the next PWM cycle. Note that immediately after the current is enabled, the voltage on the xISEN pin is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry. This blanking time also sets the minimum on-time of the PWM cycle.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor, connected to the xISEN pin, with a reference voltage. The reference voltage is derived from the voltage applied to the VREF pin and it is V_{VREF} / 6.6. The VREF pin can be tied, on board, to the 3.3 V – VINT pin, or it can be externally forced to a desired VREF voltage.
The full scale chopping current in a winding is calculated as follows:

$$I_{TRIP} = \frac{V_{VREF}}{6.6 \times R_{ISENSE}}$$

where

- I_{TRIP} is the regulated current.
- V_{VREF} is the voltage on the VREF pin.
- R_{ISENSE} is the resistance of the sense resistor.

Example : If V_{VREF} is 3.3 V and a 1 Ω sense resistor is used, the full-scale chopping current is 3.3 V / (6.6 × 1 Ω) = 0.5 A.

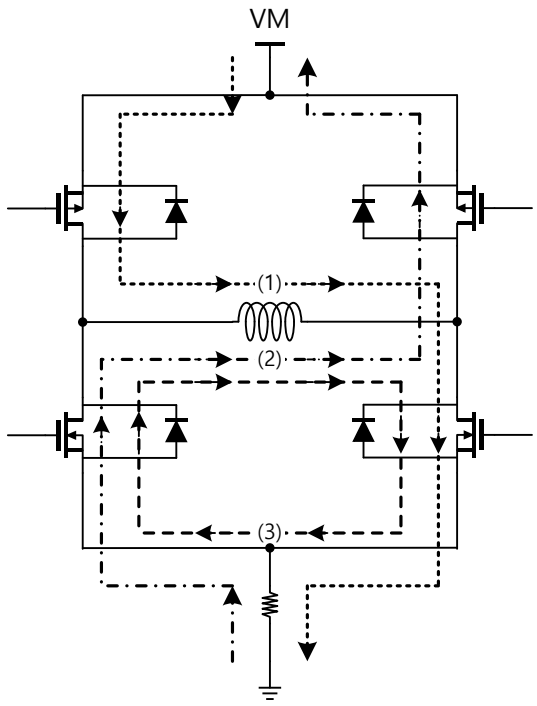
Note that if the current control is not needed, the xISEN pins may be connected directly to ground. In this case, VREF should be connected to VINT.

7.7 Current Recirculation and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached (see case 1 in Figure 7-3).

After the chopping current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, current must continue to flow for some period of time. This is called recirculation current. To handle this recirculation current, this device H-bridge operates in mixed decay mode.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the opposite drivers are turned on to allow the current to decay (see case 2 in Figure 7-3). If the winding current approaches zero, while in fast decay, the bridge is disabled to prevent any reverse current flow. In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge (see case 3 in Figure 7-3). Mixed decay starts with fast decay, then goes to slow decay. In this device, the mixed decay ratio is 25% fast decay and 75% slow decay (as shown in Figure 7-4).



(1) Drive Current
(2) Fast decay
(3) Slow decay

Figure 7-3. Decay Modes

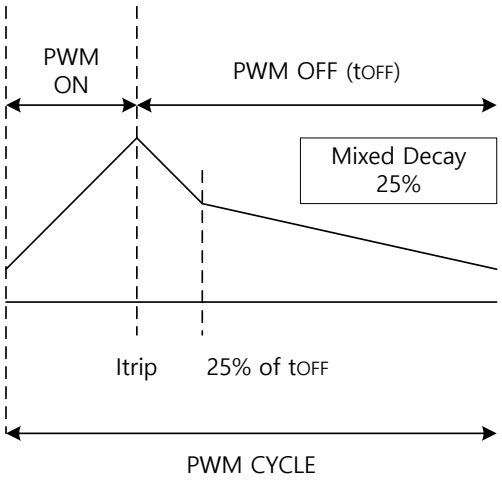


Figure 7-4. Mixed Decay

7.8 Protection Circuits

The AP8300 is fully protected against undervoltage, overcurrent, and over temperature events.

Table 7-3. Functional Modes

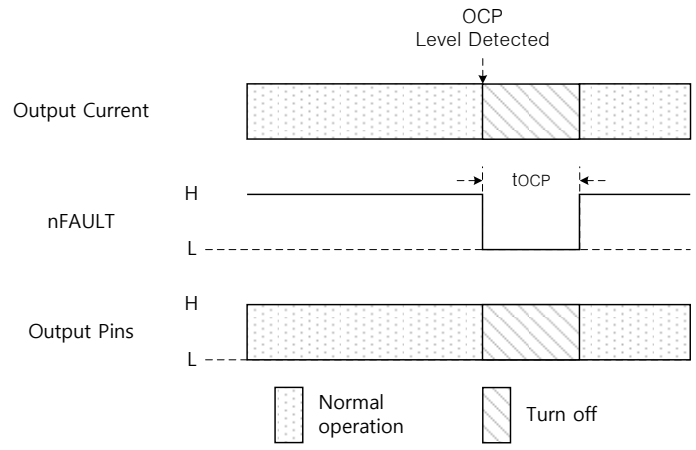
FAULT	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	nFAULT unlatched	Disabled	Shut down	System and fault clears on recovery
Overcurrent (OCP)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery and motor is driven after time, tOCP
Thermal shutdown (TSD)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery

OCP (Over Current Protection)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time tDEG, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until the retry time tOCP occurs. The OCP is implemented with a common protection architecture shared by both H-bridges.

Over current conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event. Note that OCP does not use the current sense circuitry used for PWM current control, so OCP functions even without presence of the xISEN resistors.

<OCP operation>

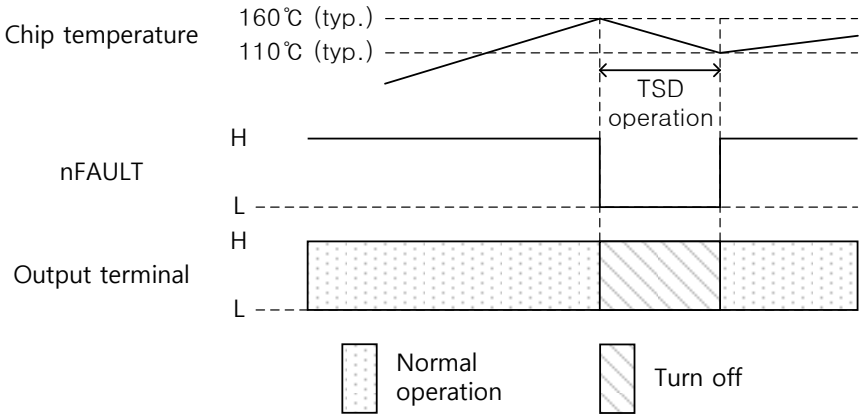


7.8 Protection Circuits (Cont.)

TSD (Thermal Shutdown)

If the die temperature exceeds T_{TSD}, all FETs in the H-bridge are disable and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed. It has a hysteresis.

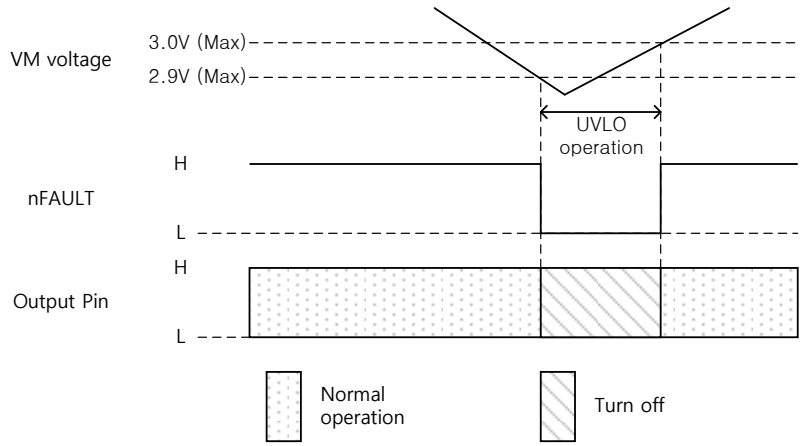
<TSD operation>



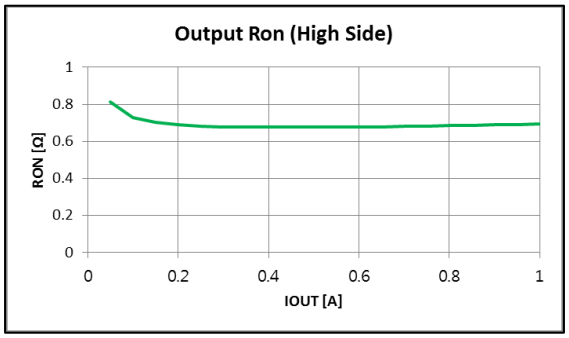
UVLO (Under Voltage Lockout)

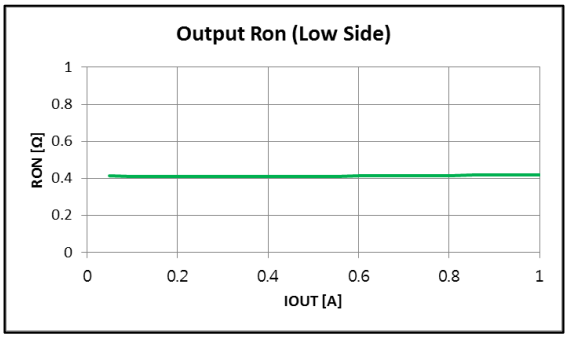
If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, VUVLO, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when VVM rises above the UVLO rising threshold. The nFAULT pin is driven low during an undervoltage condition and is released after operation has resumed.

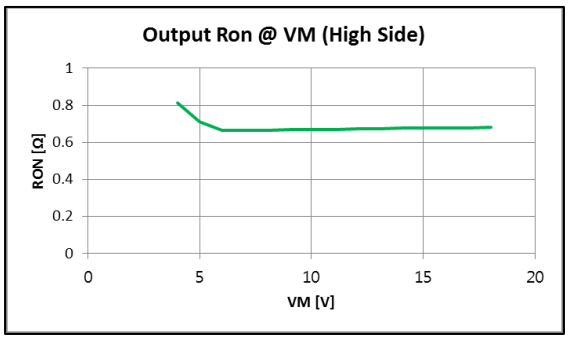
<UVLO operation>

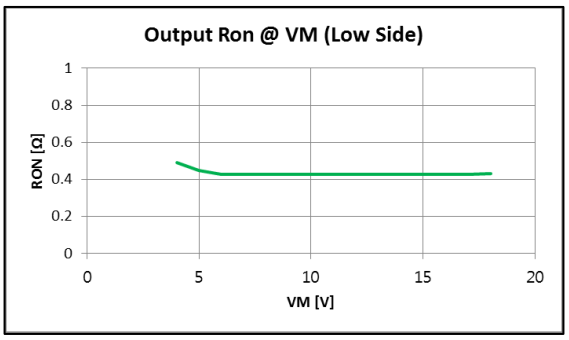


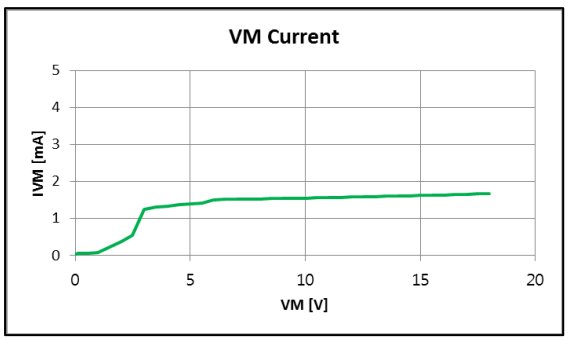
8. Typical Performance Characteristics



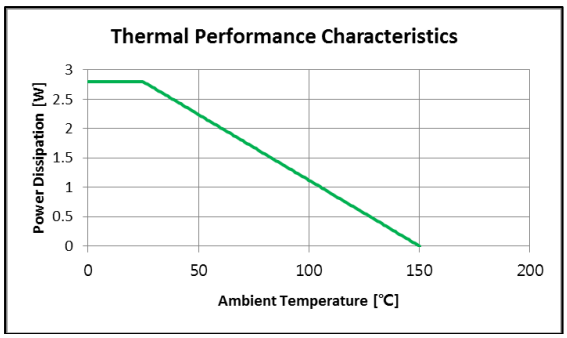








8.1 Thermal Performance Characteristics



9. Application Circuit

Information in the following application Circuits is not part of the APsemi component specification, and APsemi does not warrant its accuracy or completeness. APsemi's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Dual DC Motor Operation (Example)

If customers would like to drive two DC motors each, it recommends the following circuit.

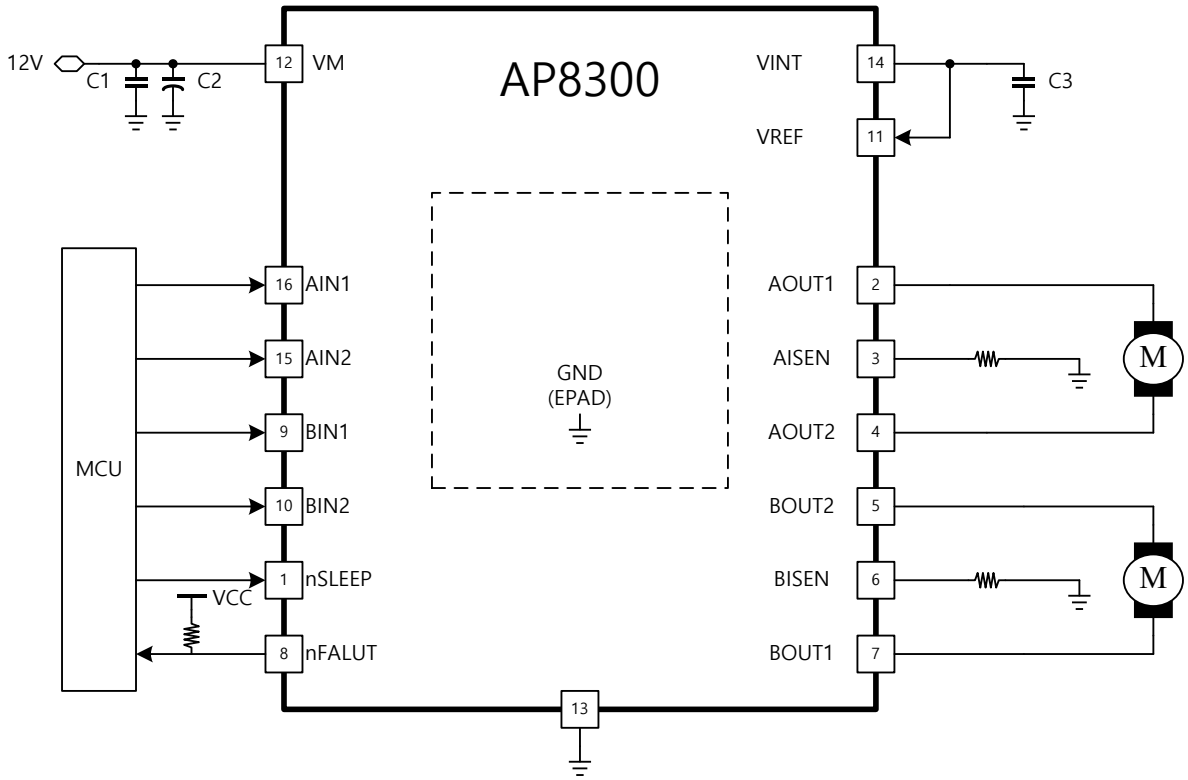


Figure 9-1. Dual DC Motor operation circuit

Example Value

. C1 : 10uF, C2=100nF, C3=2.2uF

. MCU should have six ports which is five outputs and one input.

9. Application Circuit (Cont.)

Step Motor Operation (Example)

If customers would like to drive step motor, it recommends the following circuit.

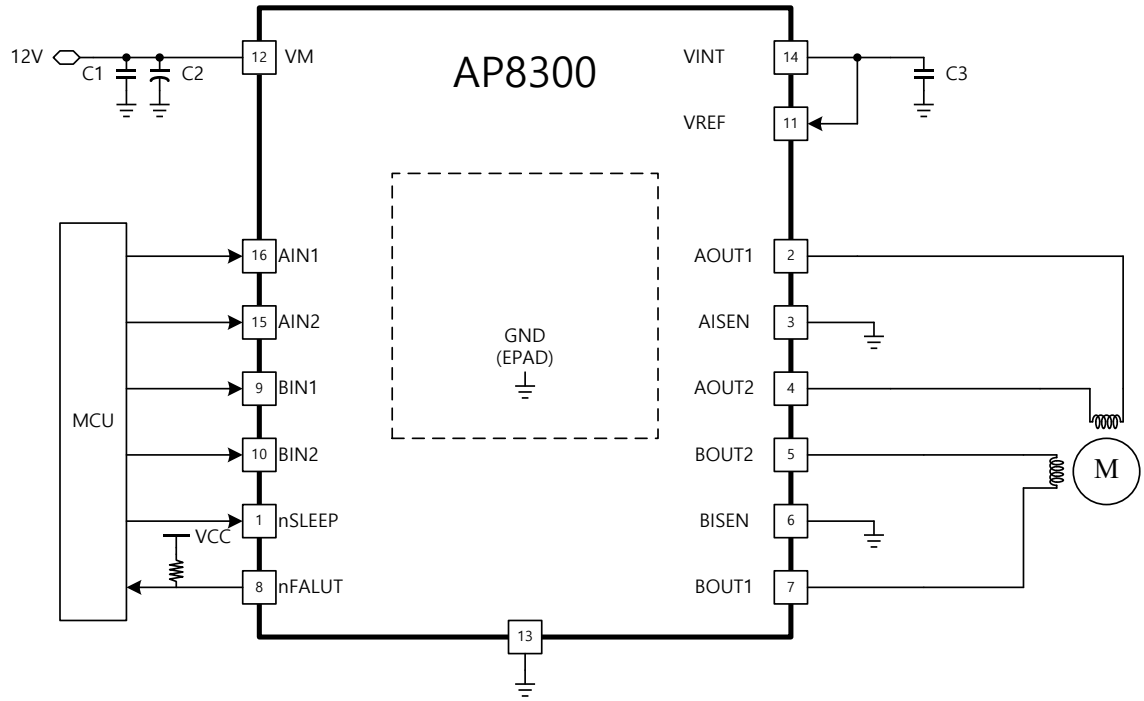


Figure 9-2. Step Motor operation circuit

Example Value

. C1 : 10uF, C2=100nF, C3=2.2uF

. MCU should have six ports which is five outputs and one input.

9. Application Circuit (Cont.)

Single DC Motor Operation (Example)

If customers would like to drive DC motor with twice the current, it recommends the following circuit.

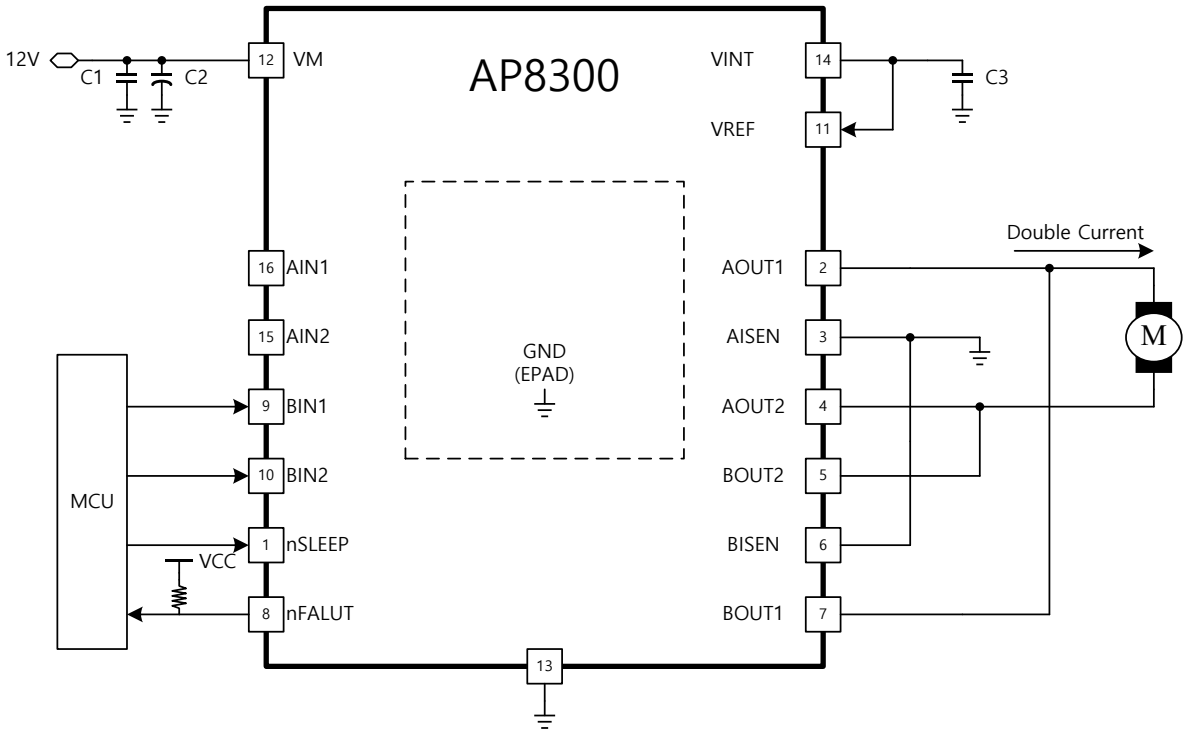


Figure 9-3. Single DC Motor operation circuit

Example Value

. C1 : 10uF, C2=100nF, C3=2.2uF

. MCU should have four ports which is three outputs and one input.

10. LAYOUT

10.1 LAYOUT Guidelines

Bypass the VM terminal to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10 μF rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

Bypass VINT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

10.2 LAYOUT Example

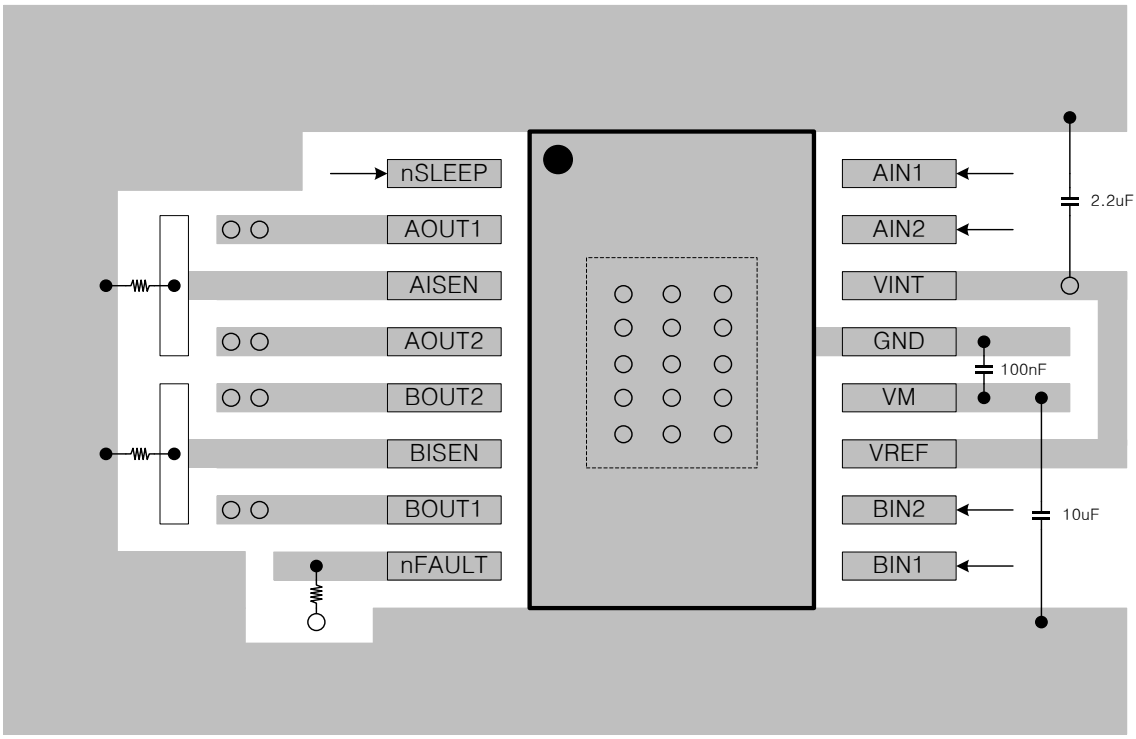


Figure 10-1. Layout Recommendation

11. Ordering Information

11.1 Packing Information

Part No	Package	Packing	Finish	Halogen	Packing Unit
AP8300L	ETSSOP-16L	4,000 pcs/REEL	Sn	Free	32,000 pcs (8 REEL)

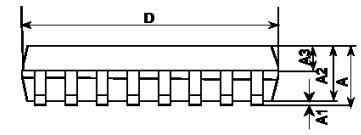
11.2 Marking Information

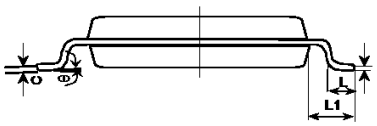
AP8300L

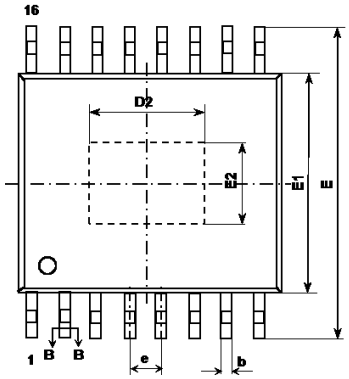
1st Line : Device name **- AP8300L : ETSSOP-16L PKG code** **2nd Line : Date code** **- YY : Last two digits of calendar year** **- WW : Work week calendar** **- Z : ASSEMBLY SITE**

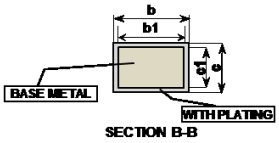
12. Package Information

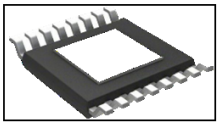
ETSSOP-16L Type (AP8300L)











SYMBOL	ETSSOP-16L Unit : mm		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
C1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	8°

Size(mm) / L/F Size (mil)	D2	E2
91x118	2.80REF	2.10REF

Appendix 1. Revision History

No	Date	Contents
Rev00	2021-07-01	Initial Datasheet Release
Rev01	2021-11-03	6.4 Electrical Characteristics fixed typos . IREF : 1uA(Typ) -> 1uA(Max)
Rev02	2021-11-23	6.4 Electrical Characteristics duplicate specification . IREF : 1uA(Typ) Delete
Rev03	2022-04-14	11.1. Packing Information Modified . Packing : 3,000 pcs/REEL => 4,000 pcs/REEL . Packing Unit : 48,000 pcs ➔ 32,000 pcs (8 REEL)
Rev04	2026-02-26	7.8. Protection Circuits fixed typos . OCP mode : independent -> Ach/Bch common protection architecture

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